What is claimed is:

1. A method of fabricating integrated circuits from a plurality of semiconductor dice, each semiconductor die defining a top side and a bottom side, the method comprising:

attaching the bottom sides of the plurality of semiconductor dice to a substrate so that the plurality of semiconductor dice are in adjacent disposition and define one or more bending regions;

creating a planar processing area for subsequent seamless high density thin film interconnect on the top sides of the plurality of semiconductor dice and the one or more bending regions so that the plurality of semiconductor dice are electrically interconnected;

removing the substrate from the bottom sides of the plurality of semiconductor dice; and

bending the thin film interconnect at the one or more bending regions so that the semiconductor dice may overlap to form a stacked plurality of semiconductor dice.

2. The method of claim 1, wherein the step of attaching the bottom sides of the plurality of semiconductor dice comprises the step of bonding the bottom sides of the semiconductor die to the substrate.

3. The method of claim 1, wherein the step of creating a planar processing area for subsequent seamless high density thin film interconnect on the top sides of the plurality of semiconductor dice and the one or more bending regions so that the plurality of semiconductor dice are electrically interconnected comprises the step of laminating a sheet of flexible dielectric material to the top sides of the plurality of semiconductor dice.

4. The method of claim 3, wherein the step of creating a thin film interconnect on the top sides of the plurality of semiconductor dice and the one or more folding regions so that the plurality of semiconductor dice are electrically interconnected further comprises the steps of:

creating vias through the sheet of flexible material down to the top sides of the plurality of semiconductor dice;

depositing a conductive material within the vias; and

forming conductive interconnection routes between the vias to create a seamless interconnection interface capable of area array connections with pad pitches from 50 to 1,000 microns.

5. The method of claim 4, wherein the flexible material is a polyimide film.

6. The method of claim 1, wherein the step of removing the substrate from the bottom sides of the plurality of semiconductor dice comprises the step of backgrinding the substrate to remove the substrate from the bottom sides of the plurality of semiconductor dice.

7. The method of claim 6, further comprising the step of backgrinding the bottom sides of the plurality of semiconductor dice to decrease the thickness of each of the plurality of semiconductor dice.

8. The method of claim 7, wherein the step of bending comprises the step of folding the thin film interconnect so that the bottom sides of at least two semiconductor dice are juxtaposed and have a stack height less than 400 microns.

9. The method of claim 8, wherein the step of folding the thin film interconnect at the one or more bending regions so that the bottom sides and top sides

overlap and then bonding with a thermally conductive adhesive to form a stacked plurality of semiconductor dice.

10. The method of claim 1, wherein the step of removing the substrate from the bottom sides of the plurality of semiconductor dice comprises the step of performing laser ablation to remove the substrate from the bottom sides of the plurality of semiconductor dice.

11. The method of claim 1, wherein the step of attaching the bottom sides of the plurality of semiconductor dice to a cavity substrate so that the plurality of semiconductor dice are in adjacent disposition within the large substrate pocket and define one or more bending regions comprises the steps of:

defining a set of semiconductor die to form a stacked plurality of semiconductor dice; and

arranging the set of semiconductor die to minimize electrical connections in the thin film interconnect; wherein multiple sets of semiconductor die define the plurality of semiconductor dice.

12. The method of claim 1, further comprising the step of creating a pad layer on a section of the thin film interconnect, wherein the pad layer overlays at least one of the plurality of semiconductor dice and is suitable for subsequent flip chip attachment and wire bond assembly.

13. The method of claim 8, wherein the step of folding the thin film interconnect at the one or more bending regions so that the top sides overlap to form a stacked plurality of semiconductor dice comprises the step of folding the thin film interconnect so that the pad layers of the dice are capacitively coupled.

14. The method of claim 12, which further comprises the step of creating another pad layer wherein the next level connection pads are placed in at least one bending region defined by a die gap and then used for subsequent electrical solder connection within the bent region of the thin film interconnect along the side of the stacked die assembly.

15. The method of claim 1, further comprising the step of singulating the plurality of semiconductor dice into sub-pluralities of semiconductor die by etching the dielectric layers along the unused sides.

16. A method of fabricating an assembly of integrated circuits, comprising:

adjacently positioning a plurality of semiconductor dice, each of the plurality of semiconductor dice having a top side and a bottom side, the top sides defining a planar processing surface and;

defining a bending region common to at least two of the plurality of semiconductor dice;

creating a flexible member on the top sides of the plurality of semiconductor dice and across the bending region;

creating flexible electrical interconnections in the flexible member to electrically connect the plurality of semiconductor dice; and

bending the flexible member at the folding region to form a multidimensional interconnected dice structure.

17. The method of claim 16, wherein the step of bending comprises the step of bending the flexible member at the die gap regions so that the plurality of semiconductor dice define a geometric volume.

18. The method of claim 16 wherein the step of bending at the die gap region defines an angle between the two die within a range of 0 to 360 degrees.

19. An integrated circuit, comprising:

a plurality of semiconductor dice, each of the semiconductor die defining a top side and a bottom side, the top side of each semiconductor die including electrically conductive terminals, the plurality of semiconductor dice arranged to form a multidimensional interconnected dice structure; and

a flexible thin film interconnect deposited on the top sides of the plurality of semiconductor dice and comprising a plurality of flexible electrical interconnections electrically connecting the electrically conductive terminals of the plurality of semiconductor dice, the flexible thin film interconnect folded in a region defined by a pair of adjacently connected die so that the plurality of semiconductor dice form the multidimensional interconnected dice structure.

20. The integrated circuit of claim 19, wherein the bottom sides of at least two semiconductor dice are juxtaposed to the top side of another semiconductor die.

21. The integrated circuit of claim 19 wherein the multidimensional interconnected dice structure is a vertical die stack and wherein the first pad layer defines a bottom surface of the vertical die stack suitable for use in flip chip assembly

22. The integrated circuit of claim 19 wherein the multidimensional interconnected dice structure is a vertical die stack and wherein the first pad layer defines a side surface of the vertical die stack, and wherein the side surface is defined by at least one of the folded regions of the flexible thin film interconnect.

23. The integrated circuit of claim 19, wherein the flexible thin film interconnect extends from one or more die sides beyond a perimeter of the die.

24. The integrated circuit of claim 21, wherein the first pad layer defines a bottom surface of the vertical die stack and a second section of the flexible thin film interconnect defines a second top pad layer for surface mount components.

25. An integrated circuit, comprising:

a plurality of semiconductor dice, each of the semiconductor die defining a top side and a bottom side, the top side of each semiconductor die including electrically conductive terminals, the plurality of semiconductor dice arranged in an overlapping relationship to form a multidimensional interconnected dice structure; and

a flexible thin film interconnection for electrically connecting the electrically conductive terminals of the plurality of semiconductor dice, the flexible electrical interconnection deposited on the top sides of the semiconductor die and bent in a region defined by a pair of adjacently connected die so that the plurality of semiconductor dice form a multidimensional interconnected dice structure that can be further electrically connected to selected top, side and bottom defined thin film pads using standard assembly processes.